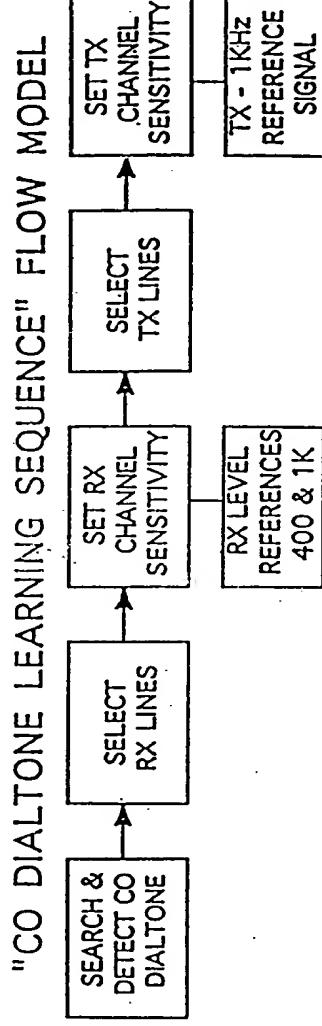


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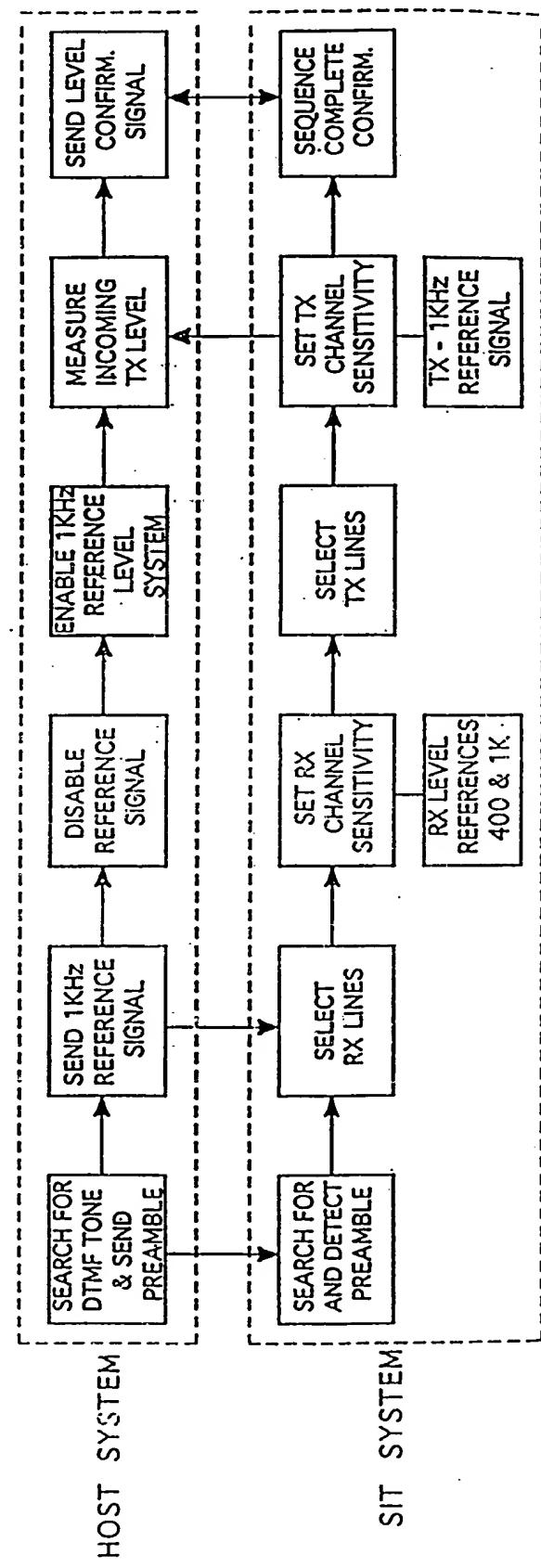
5892823

S.N. 08/625398  
A.U. 2742  
1-8



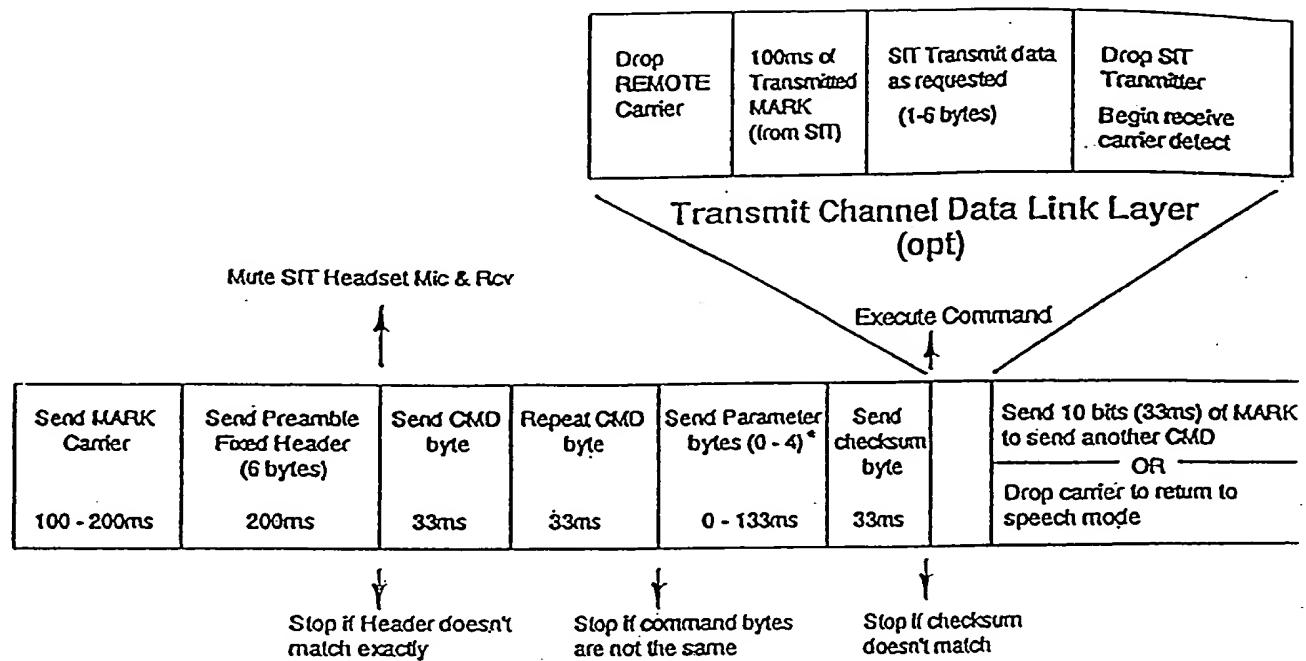
**FIG. 1**

"AUTOMATED 800 LEARNING SEQUENCE" FLOW MODEL



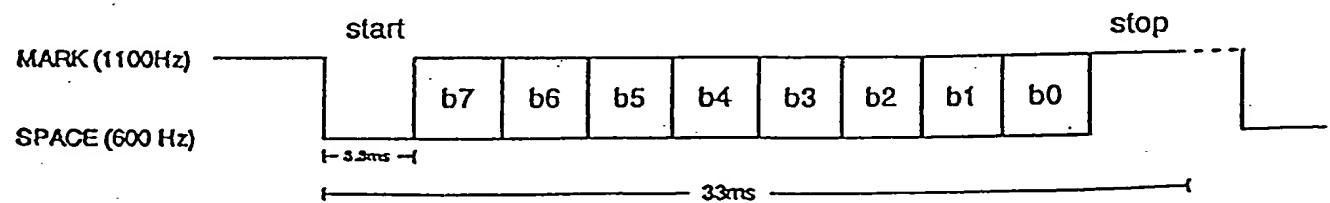
**FIG. 2**

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NOTE: The number of parameters is directly dependent on the Command type

### Receive Channel Data Link Layer

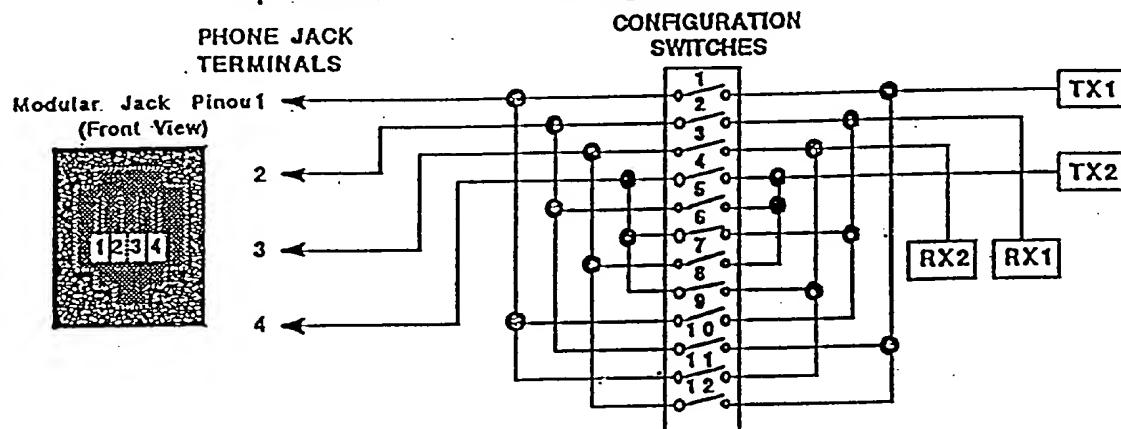


### Receive Channel Physical Layer

**FIG. 3**

**Smart Interface Technology (SIT) Project**  
**Preliminary Line Configuration Switching Algorithms and Model**

**Equivalent Line Configuration Switching Model**



<u>Dialtone Detection</u>	<u>Rx Pinout</u>	<u>Tx Pinout Sequence*</u>	<u>Algorithm Ref. No.</u>	<u>Model Sw. "ON"</u>
Pins 2 & 3	Pins 2 & 3	Pins 1 & 4 (Primary)	1	1,2,3,4
Pins 2 & 3	Pins 2 & 3	Pins 1 & 2 (2nd Try)	2	1,2,3,5
Pins 2 & 3	Pins 2 & 3	Pins 1 & 3 (3rd Try)	3	1,2,3,7
Pins 2 & 3	Pins 2 & 3	Pins 4 & 2 (4th Try)	4	2,3,4,10
Pins 2 & 3	Pins 2 & 3	Pins 4 & 3 (5th Try)	5	2,3,4,12
Pins 2 & 4	Pins 2 & 4	Pins 1 & 3 (Primary)	6	1,2,7,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 2 (2nd Try)	7	1,2,5,8
Pins 2 & 4	Pins 2 & 4	Pins 1 & 4 (3rd Try)	8	1,2,4,8
Pins 2 & 4	Pins 2 & 4	Pins 3 & 2 (4th Try)	9	2,5,8,12
Pins 2 & 4	Pins 2 & 4	Pins 3 & 4 (5th Try)	10	2,4,8,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 4 (Primary)	11	2,4,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 1 (2nd Try)	12	1,2,11,12
Pins 1 & 2	Pins 1 & 2	Pins 3 & 2 (3rd Try)	13	2,5,11,12
Pins 1 & 2	Pins 1 & 2	Pins 4 & 1 (4th Try)	14	1,2,4,11
Pins 1 & 2	Pins 1 & 2	Pins 4 & 2 (5th Try)	15	2,4,10,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 4 (Primary)	16	3,4,9,11
Pins 1 & 3	Pins 1 & 3	Pins 2 & 1 (2nd Try)	17	1,3,5,9
Pins 1 & 3	Pins 1 & 3	Pins 2 & 3 (3rd Try)	18	3,5,9,12
Pins 1 & 3	Pins 1 & 3	Pins 4 & 1 (4th Try)	19	1,3,4,9
Pins 1 & 3	Pins 1 & 3	Pins 4 & 3 (5th Try)	20	3,4,9,12

**FIG. 4**

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<u>Dialtone Detection</u>	<u>Rx Pinout</u>	<u>Tx Pinout Sequence</u>	<u>Algorithm Ref. No.</u>	<u>Model Sw. "ON"</u>
Pins 1 & 4	Pins 1 & 4	Pins 2 & 3 (Primary)	21	7,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 2 & 1 (2nd Try)	22	1,5,8,9
Pins 1 & 4	Pins 1 & 4	Pins 2 & 4 (3rd Try)	23	4,8,9,10
Pins 1 & 4	Pins 1 & 4	Pins 3 & 1 (4th Try)	24	1,7,8,9
Pins 1 & 4	Pins 1 & 4	Pins 3 & 4 (5th Try)	25	4,8,9,12
Pins 3 & 4	Pins 3 & 4	Pins 1 & 2 (Primary)	26	1,3,5,6
Pins 3 & 4	Pins 3 & 4	Pins 1 & 3 (2nd Try)	27	1,3,6,7
Pins 3 & 4	Pins 3 & 4	Pins 1 & 4 (3rd Try)	28	1,3,4,6
Pins 3 & 4	Pins 3 & 4	Pins 2 & 3 (4th Try)	29	3,6,7,10
Pins 3 & 4	Pins 3 & 4	Pins 2 & 4 (5th Try)	30	3,4,6,10

<u>ALGORITHM REF. NUMBER</u>	<u>SWITCHING MODEL ACTION</u>	<u>ALGORITHM REF. NUMBER</u>	<u>SWITCHING MODEL ACTION</u>
31	Switch 1: "ON"	43	Switch 7: "ON"
32	Switch 1: "OFF"	44	Switch 7: "OFF"
33	Switch 2: "ON"	45	Switch 8: "ON"
34	Switch 2: "OFF"	46	Switch 8: "OFF"
35	Switch 3: "ON"	47	Switch 9: "ON"
36	Switch 3: "OFF"	48	Switch 9: "OFF"
37	Switch 4: "ON"	49	Switch 10: "ON"
38	Switch 4: "OFF"	50	Switch 10: "OFF"
39	Switch 5: "ON"	51	Switch 11: "ON"
40	Switch 5: "OFF"	52	Switch 11: "OFF"
41	Switch 6: "ON"	53	Switch 12: "ON"
42	Switch 6: "OFF"	54	Switch 12: "OFF"

**NOTES:**

- 1) Algorithm No. 1 will be the default setting for system power-up, hard or soft resets and "learning" timeout conditions.
- 2) Ideally all 12 equivalent switches can be selected and switched "on" or "off" independant of the above algorithm's.

**FIG. 5**

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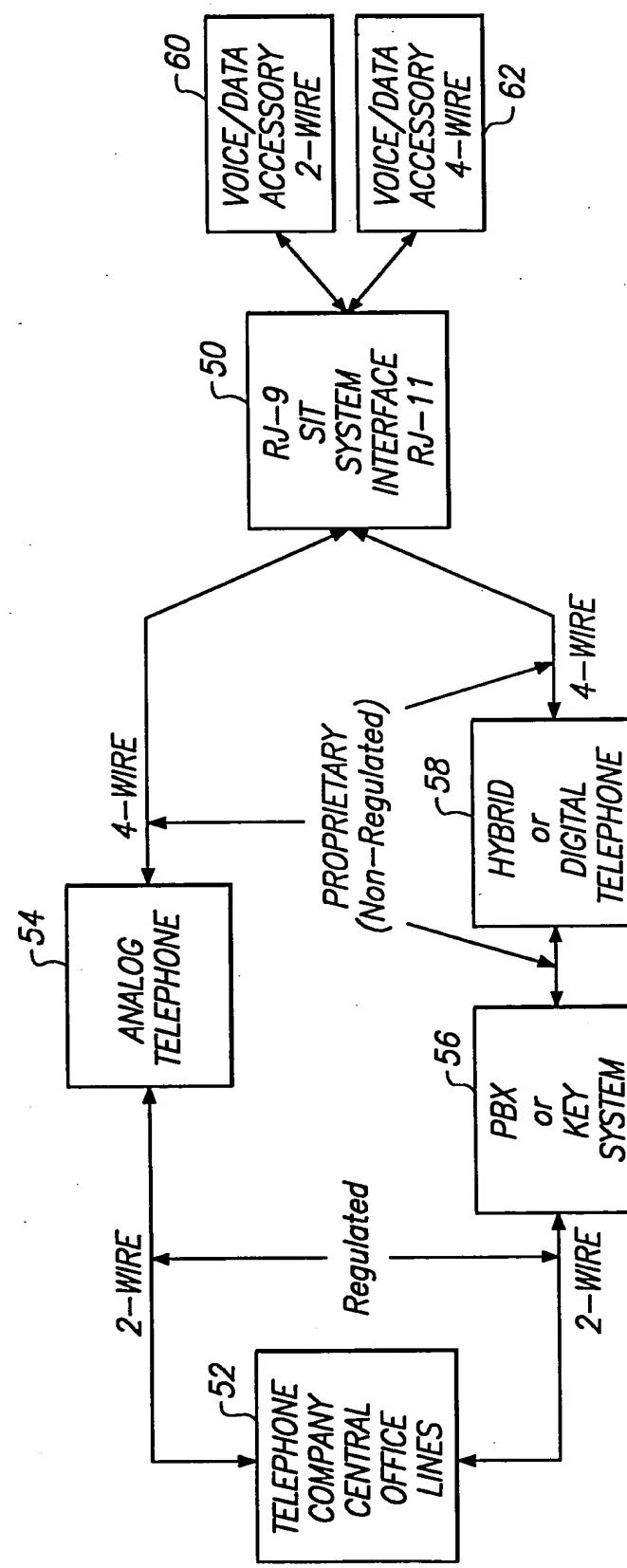
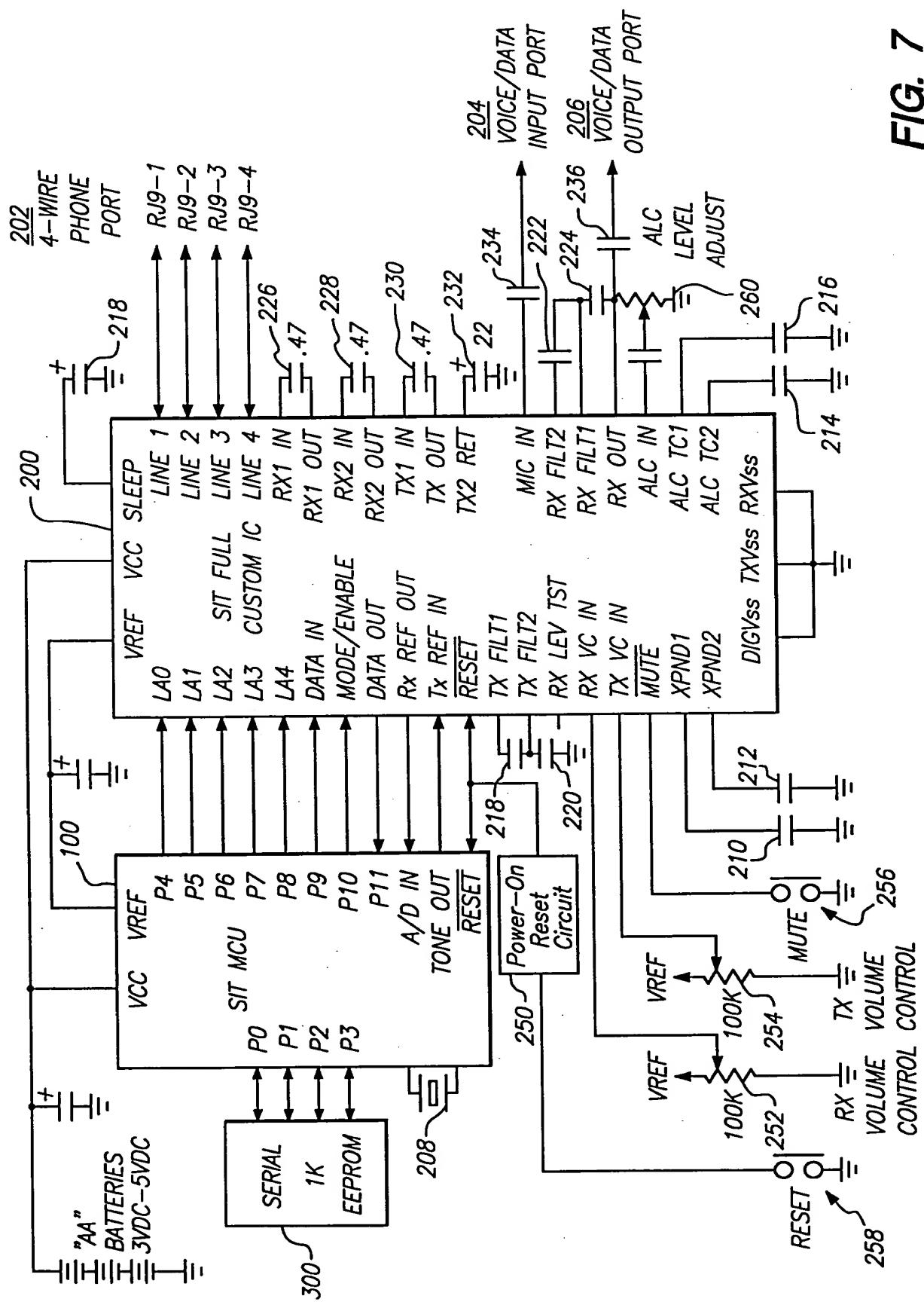
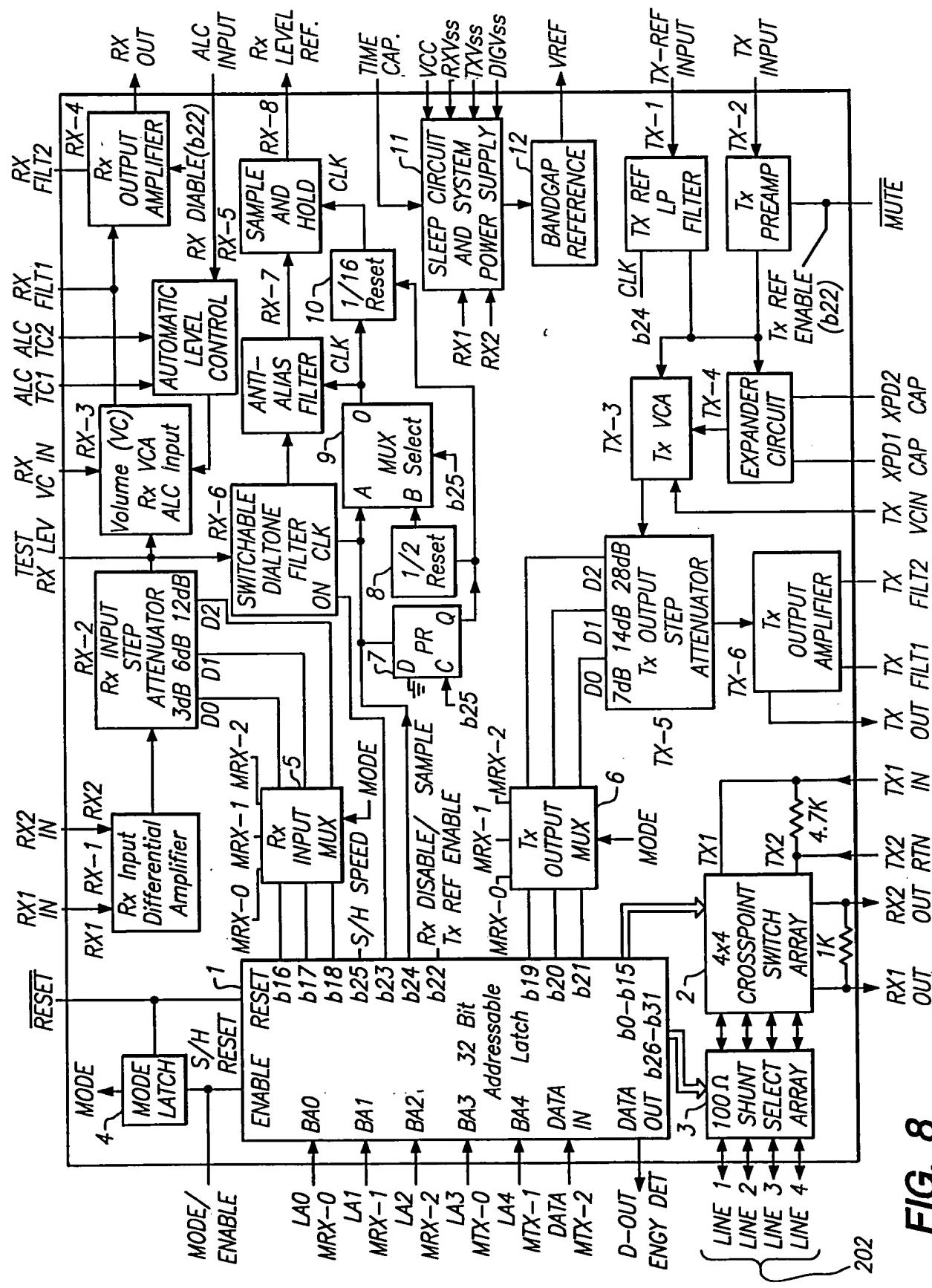
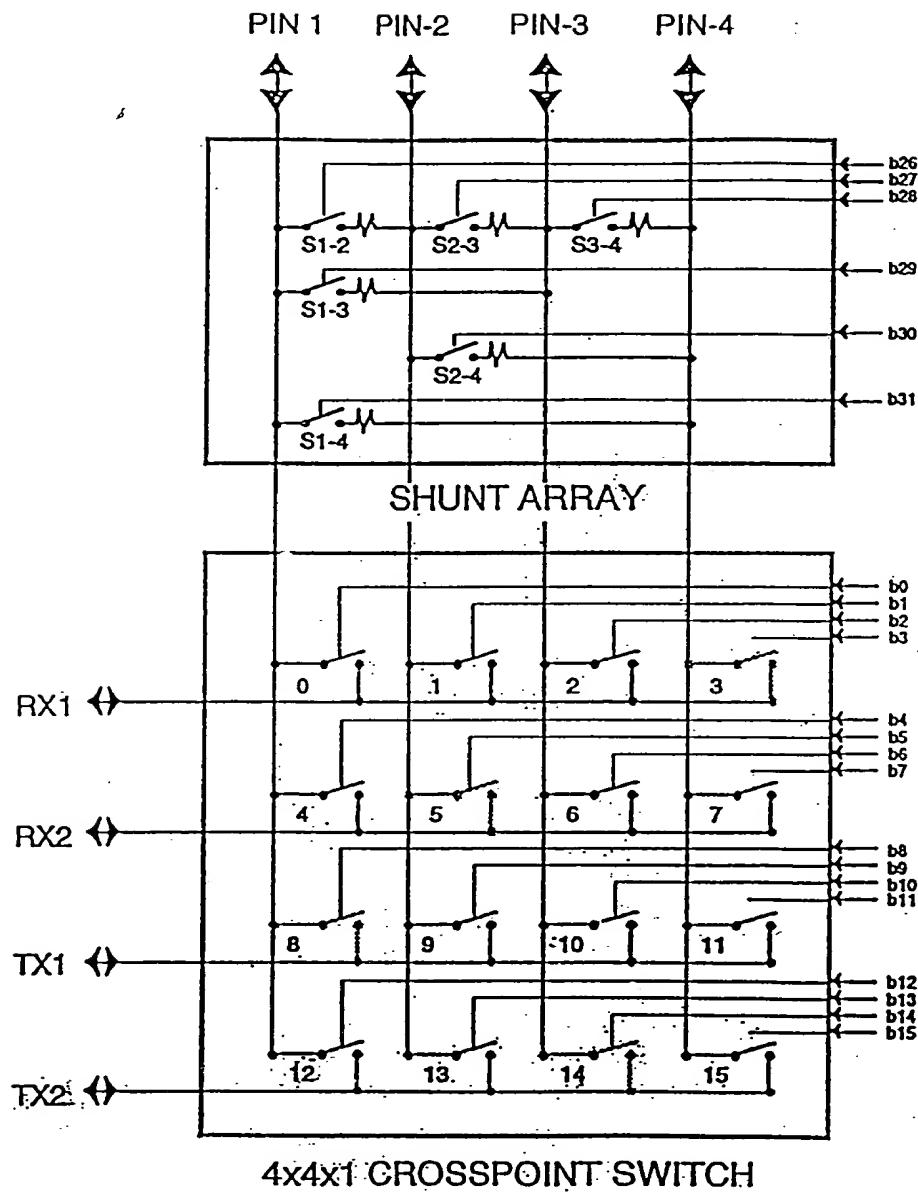


FIG. 6





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DRAFTSMAN	SUBCLASS



**FIG. 9**